S Y L L A B U S

General information	**Title and code of subject, number of credits**	CMS 363 Digital Logic, 8 ECTS	
	Department	Computer Science	
	Program	Bachelor	
	Academic semester	Spring 2024	
	Lecturer	M.Sc Babak Emdadi	
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	Lecture room/Schedule	11 Mehseti Street, AZ1096 Baku, Azerbaijan (Neftchilar campus)	
	Consultations	As Scheduled	
Course language	English		
Type of the subject	Major		
Textbooks and additional materials	***Textbooks*:** 1. Fundamentals of digital logic with Verilog design, 3rd Edition, (2014) by S.D. Brown, Tata McGraw-Hill Education. (required) Optional Reference Texts: 2. Fundamentals of digital logic with Verilog design, 2nd Edition, (2007) by S.D. Brown, Tata McGraw-Hill Education. Additional Resource Texts: 3. Digital logic design using verilog: coding and RTL synthesis (2016) by Taraate Vaibbhav, Springer. 4. Digital Logic Design Principles, (2007) by N. Balabanian, B. Carlson, Wiley India Pvt. Limited. 5. Digital Principles and Logic Design, (2007) by A. Saha, N. Manna, Infinity Science Press LLC. **Auxiliary Web sources:** https://www.youtube.com/watch?v=M0mx8S05v60&list=PLBlnK6fEyqRjMH3mWf6kwqiTbT798eAOm https://www.youtube.com/watch?v=j4fDYX5VZF0&list=PLEbnTDJUr_Ica5kK6UypsWpf95Ut2sK3o https://www.youtube.com/watch?v=La9Nk6iwHvU&list=PLdNU3YZoxOwsx4YL3Grfixt1wNOZjOpyS https://www.youtube.com/watch?v=QSEl_O0Gtoo&list=PLoM0uG7tqR3qVss3zhBRniXU7mhHy2bwj		
Teaching methods	**Lecture**		X
	Group discussion		X
Assessment	**Components**	**Date/ Deadline**	**Percent (%)**
	Quizzes	During the semester, 2 quizzes	10
	Active participation	During the semester	10
	Attendance	At each lesson	10
	Midterm exam		30
	Final exam		40
	Final		**100**
Course description	This subject teaches main principles of digital logic. It introduces the essential steps in the design process and discussed how CAD (Computer-Aided Design) tools can be used. Moreover, it explains the concepts of logic circuit synthesis and optimization, and describes how Verilog can be used to specify the desired functionality and how CAD tools provide a mechanism for developing the required circuits. This course also presents combinational circuits that are used as building blocks which includes the encoder, decoder, and multiplexer circuits. Using above mentioned circuits the application of different Verilog constructs will be illustrated. It gives the students an opportunity to discover more advanced features of Verilog. Lastly, storage elements and synchronous sequential circuits will be analyzed and described in detail.		
Course objectives	The main objective of this course as follow: 1. To be able to perform the conversion among different number systems;		

	2. To familiarize with logic gates - AND, OR, NOT, NAND, NOR, XOR. 3. To understand basic properties of Boolean algebra, able to simplify simple Boolean functions. 4. To be able to design simple combinational logics using basic gates. 5. To be able to optimize simple logic using Karnaugh maps. 6. To familiarize with SR lutch, D Flip-Flop and their usage and able to analyze sequential logic circuits. 7. To understand finite state machines (FSM) concept. 8. To familiarize with basic combinational and sequential components circuits. 9. To be able to understand and use one high-level hardware description languages (Verilog) to design combinational or sequential circuits.
Learning outcomes	What students should know by the end of the course: Concept of digital and binary systems, to design and analyze logic circuits, basic software tools for the design and implementation of digital circuits and systems.
Rules (Educational policy and behavior)	▪ **Preparation for class** The structure of this course makes your individual study and preparation outside the class extremely important. The lecture material will focus on the major points introduced in the text.Reading the assigned chapters and having some familiarity with them before class will greatly assist your understanding of the lecture. After the lecture, you should study your notes and work relevant problems and cases from the end of the chapter and sample examquestions. • **Withdrawal (pass/fail)** This course strictly follows grading policy of the School of Humanities, Education and Social sciences. Thus, a student is normally expected to achieve a mark of at least 60% to pass. In case of failure, he/she will be required to repeat the course thefollowing term or year. ▪ **Cheating/plagiarism** Cheating or other plagiarism during the Quizzes, Mid-term and Final Examinations will lead to paper cancellation. In this case, the student will automatically get zero (0), without any considerations. ▪ **Professional behavior guidelines** The students shall behave in the way to create favorable academic and professionalenvironment during the class hours. Unauthorized discussions and unethical behavior are strictly prohibited. **Attendance** Students who attend the whole classes will get 10 marks. For two absence (one week) student loses 1 mark. • **Quizzes** There will be two quizzes during the semester. The quizzes will be announced in the classroom one weeks before and will relate to homework. • **Activity** Students who will be active during discussion of past lessons and laboratory classes will be awarded activity mark. During the semester, various exercises will be solved on the subjects taught by the students, so they can get full marks.

This program reflects the comprehensive information about the subject and information about any changes will be provided in advance.

Week	Dates (planned)	Subject topics	Textbook/ Assignments
1		***Lecture №1.*** *Introduction:* Digital hardware. The design process. Structure of a computer. Logic circuit design in this book. Digital representation of information. Binary numbers. Conversion between decimal and binary systems. ASCII character code. Digital and analog information.	[1] p. 1-16
2		***Lecture №2.*** *Introduction to logic circuits:* Variables and functions. Inversion. Truth tables. Logic gates and networks. Analysis of a logic network. Boolean algebra. The venn diagram. Notation and terminology. Precedence of operations. Synthesis using and, or, and not gates. Sum-of-products and product-of-sums forms. NAND and NOR logic networks. Design examples. Three-way light control. Multiplexer circuit. Number display	[1] p. 21-63
3		***Lecture №3****. Introduction to logic circuits:* Introduction to CAD tools. Design entry. Logic synthesis. Functional simulation. Physical design. Timing simulation. Circuit implementation. Complete design flow. Introduction to Verilog. Structural specification of logic circuits. Behavioral specification of logic circuits. Hierarchical verilog code. How *not* to write verilog code.	[1] p. 63-78
4		***Lecture №4.*** *Introduction to logic circuits:* Minimization and karnaugh maps. Strategy for minimization. Terminology. Minimization procedure. Minimization of product-of-sums forms. Incompletely specified functions. Multiple-output circuits.	[1] p. 78-101

5		**Lecture №5**. *Implementation Technology*: Transistor. NMOS Logic Gates. CMOS Logic Gates. Speed of Logic Gate Circuits. Negative Logic System. Standard Chips. 7400-Series Standard Chips. Programmable Logic Devices. Programmable Logic Array (PLA). Programmable Array Logic (PAL). Programming of PLAs and PALs. Complex Programmable Logic Devices (CPLDs). Field-Programmable Gate Arrays. Custom Chips, Standard Cells, and Gate Arrays. Practical Aspects. Fabrication and Behavior. On-Resistance. Voltage Levels in Logic Gates. Noise Margin. Dynamic Operation of Logic Gates. Power Dissipation in Logic Gates.Passing 1s and 0s Through Transistor Switches.Transmission Gates.	[1] p. 733-786
6		***Lecture №6.*** *Number Representation and Arithmetic Circuits:* Positional number representation. Unsigned integers. Octal and hexadecimal representations. Addition of unsigned numbers. Decomposed full-adder. Ripple-carry adder. Design example. Signed numbers. Negative numbers. Addition and subtraction. Adder and subtractor unit. Radix-complement schemes. Arithmetic overflow. Performance issues. Fast Adders. Carry-lookahead adder.	[1] p. 122-151
7		***Lecture №7.*** *Number Representation and Arithmetic Circuits:* Design of arithmetic circuits using CAD tools. Design of arithmetic circuits using schematic capture. Design of arithmetic circuits using Verilog. Using vectored signals. Using a generic specification. Nets and variables in verilog. Arithmetic assignment statements. Module hierarchy in verilog code. Representation of numbers in verilog code. Multiplication. Array multiplier for unsigned numbers. Multiplication of signed numbers. Other number representations. Fixed-point numbers. Floating-point numbers. Binary-coded-decimal representation.	[1] p. 151-178
8		***Lecture №8***. *Combinational-circuit building blocks:* Multiplexers. Synthesis of logic functions using multiplexers. Multiplexer synthesis using Shannon's expansion. Decoders. DE multiplexers. Encoders. Binary encoders. Priority encoders. Code converters. Arithmetic comparison circuits. For combinational circuits. Conditional operator. If-else statement. The case statement. The for loop. Verilog operators. The generate construct. Tasks and functions.	[1] p. 189-232
9	***Midterm exam***		
10		***Lecture №9.*** *Flip-flops, registers, and counters:* Basic latch. Gated SR latch. Gated SR latch with NAND gates. Gated D latch. Effects of propagation delays. Edge-triggered D flip-flops. Master-slave D flip-flop. Other types of edge-triggered D flip-flops. D flip-flops with clear and present. Flip-flop timing parameters. T flip-flop. Jk Flip-flop. Summary of terminology.	[1] p. 247-267
11		***Lecture №10.*** *Flip-flops, registers, and counters:* Registers. Shift register. Parallel-access shift register. Counters. Asynchronous counters. Synchronous counters. Counters with parallel load. Reset synchronization. Other types of counters. BCD counter. Ring counter. Johnson counter. Remarks on counter design.	[1] p. 267-283
12		***Lecture №11.*** *Flip-flops, registers, and counters:* Using storage elements with CAD tools. Including storage elements in schematics. Using Verilog constructs for storage elements. Blocking and non-blocking assignments. Non-blocking assignments for combinational circuits. Flip-flops with clear capability. Using Verilog constructs for registers and counters. Flip-flops and registers with enable inputs. Shift registers with enable inputs. Design example. Reaction timer. Register transfer level (RTL) code. Timing analysis of flip-flop circuits. Timing analysis with clock skew.	[1] p. 283-314
13		***Lecture №12.*** *Synchronous sequential circuits:* Basic design steps. State diagram. State table. State assignment. Choice of flip-flops and derivation of next-state and output expressions. Timing diagram. Summary of design steps. State-assignment problem. One-hot encoding. Mealy state model. Design of finite state machines using CAD tools. Verilog code for moore-type FSMS. Synthesis of Verilog code. Simulating and testing the circuit. Alternative styles of Verilog code. Summary of design steps when using cad tools. Specifying the state assignment in Verilog code. Specification of mealy FSMS using verilog.	[1] p. 331-363
14		***Lecture №13.*** *Synchronous sequential circuits:* Serial adder example. Mealy-type FSM for serial adder. Moore-type FSM for serial adder. Verilog code for the serial adder. Minimization. Partitioning minimization procedure. Incompletely specified FSMS. Design of a counter using the sequential circuit approach. State diagram and state table for a modulo-8 counter. State assignment. Implementation using D-type flip-flops. Implementation using JK-type flip-flops. Example—a different counter.	[1] p. 363-393

15		***Lecture №14.*** *Synchronous sequential circuits:* FSMS ss an arbiter circuit. Analysis of synchronous sequential circuits. Algorithmic state machine (ASM) charts. Formal model for sequential circuits.	[1] p. 393-405
		Final Exam	

Babak Emdadi